CLAIMS

What is claimed is:

1. A circuit, comprising:

a n-channel differential amplifier having a first input transistor and a second input transistor that delivers current to a summing node, wherein the first and the second input transistors receive bias currents; and

a first n-channel common source amplifier and a second n-channel common source amplifier coupled to the n-channel differential amplifier, wherein the first and the second common source amplifiers have a first output and a second output to provide a negative common mode feedback that is coupled to the summing mode.

2. The circuit of claim 1, wherein the n-channel differential amplifier has a common mode output voltage.

3. The circuit of claim 2, further comprising:

a level shifter circuit coupled to the differential amplifier to adjust the first common mode output voltage.

4. The circuit of claim 2, further comprising:

a feedback circuit coupled to the first and the second outputs of the n-channel common source amplifier circuits, wherein the feedback circuit provides more current to the summing node if voltages at the first and the second outputs rise above a common mode reference voltage.

5. The circuit of claim 4, further comprising:

a biasing circuit coupled to the feedback circuit and the n-channel differential amplifier, wherein the biasing circuit provides a constant current to the summing node.

6. The circuit of claim 5, wherein the bias currents through the first and the second input transistors are reduced if a common mode voltage at the first and the second outputs rise above a common mode reference voltage.

7. The circuit of claim 6, wherein the common mode output voltage of the n-channel differential amplifier increases if the bias currents through the first and the second input transistors are reduced.

8. The circuit of claim 7, wherein the common mode output voltage of the first and the second common source amplifiers is reduced if the common mode output voltage of the n-channel differential amplifier increases.

9. The circuit of claim 1, wherein the n-channel differential amplifier, the first n-channel common source amplifier, and the second n-channel common source amplifier comprise transistors having gate widths less than or equal to 0.25 micron.

10. An operational amplifier, comprising:

a first gain stage having an inverting common mode gain, wherein the first gain stage comprises a first input transistor coupled to a summing node and a second input transistor coupled to the summing node, wherein the first gain stage outputs a common mode voltage; and

a second gain stage coupled to the first gain stage, wherein the second

gain stage provides a negative common mode feedback to the first gain stage, wherein the second gain stage outputs a common mode voltage, wherein the second gain stage comprises a first output signal and a second output signal, wherein current supplied to the summing node through the first and the second transistors is decreased if the common mode output voltage of the second gain stage is increased.

11. The operational amplifier of claim 10, further comprising:

a biasing circuit coupled to the summing node, wherein the biasing circuit sinks a constant current from the summing node.

12. The operational amplifier of claim 10, wherein the common mode output voltage of the first gain stage is increased if the current supplied to the summing node through the first and the second transistors is decreased.

13. The operational amplifier of claim 12, wherein the common mode output voltage of the second stage is decreased if the common mode output voltage of the first stage is increased.

14. The operational amplifier of claim 10, wherein the feedback is coupled to an input transistor that is connected to the summing node.

15. A operational amplifier, comprising:

means for providing a first gain stage and a second gain stage; and

means for providing a negative feedback; and

16. The operational amplifier of claim 15, further comprising:

means for implementing the operational amplifier in a 0.25 micron technology.

17. A method, comprising:

adding current to summing node using a differential pair if a common-mode voltage rises above a reference voltage;

subtracting a constant current from the summing node; and

adding a bias current to the summing mode through a first input transistor and a second input transistor.

18. The method of claim 17, further comprising:

increasing a common mode output current of a first gain stage.

19. The method of claim 18, further comprising:

reducing a common mode output current of a second gain stage.

20. The method of claim 19, wherein a common mode output voltage of the second gain stage is approximately equal to the reference voltage.

21. The method of claim 20, wherein the feedback directly feeds a node coupled to the input stage.